EasyChair Preprint

№ 7277

An Ultra-Low Power 22nm Self-Oscillating Voltage Doubler with Dynamic Leakage-Suppression Logic

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December 28, 2021

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***Abstract*— This paper presents a new structure of a self-oscillating voltage doubler (SOVD) that has a very low power. In the proposed SOVD structure, the inverters present in the old structure of an SOVD are replaced with a dynamic leakage-suppression logic inverter to reduce power consumption. When simulated under the condition of an input voltage of 300 mV, the leakage current and oscillation frequency can be reduced, resulting in extremely low power consumption. The input voltage conversion efficiency was 89.5%. The power efficiency was about 7 times higher than that of a conventional SOVD.**

Keywords—energy harvesting, voltage doubler, dynamic leakage-suppression, low power consumption.

I. INTRODUCTION

Recently, the demand for sub-millimeter-scale self-powered devices has been increasing owing to the prevalence of IoT. As a method of self-powering on the nm CMOS process, studies on energy harvesting are being actively conducted worldwide. Energy harvesting is a technology that drives devices with low power obtained from a specific power cell, such as a photodiode and glucose fuel cell. Earlier studies have shown that the power cells output a voltage of approximately 200 mV to 400 mV, depending on the surrounding environment (reference [1], [2]). However, these voltages are not sufficient to drive the circuits; for example, the LC power oscillator requires 1 V to drive itself (reference [3]). Moreover, the harvested power is very small. Therefore, to drive the circuits by energy harvesting, it is essential to boost the voltage with a considerably low power consumption.

The self-oscillating voltage doubler (SOVD) is a circuit capable of that operation, and the basic structure of an SOVD based on a standard 180 nm CMOS technology is demonstrated by [4]. Currently, CMOS manufacturing processes are further miniaturized compared to 180 nm CMOS technology, and our laboratory has introduced a minimum of 22 nm CMOS technology. However, as the leakage current of the MOSFET increases with the miniaturization of the process, the power loss becomes large, and it becomes difficult to drive circuits with low power, such as harvested power. Therefore, to design an SOVD for such an advanced process, it is essential to reduce the leakage current. This paper presents the optimal design of an SOVD based on a standard 22 nm CMOS technology.

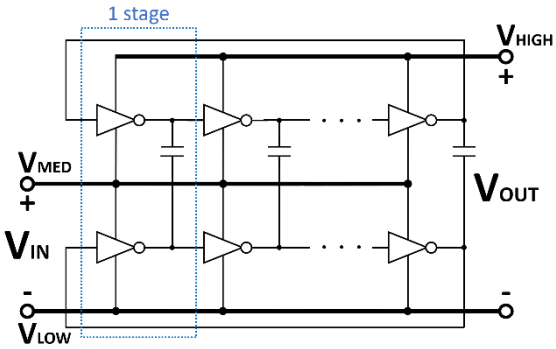

Fig. 1. Basic structure of a conventional SOVD

II. SELF-OSCILLATING VOLTAGE DOUBLER

A. Conventional structure

An SOVD can boost the input voltage and generate a clock signal simultaneously. Fig. 1 presents the circuit diagram of a conventional SOVD, which is demonstrated in [4]. As shown in Fig. 1, the SOVD consists of two stacked ring oscillators using basic CMOS inverters. The top and bottom ring oscillators are connected by a structure called a switched capacitor network that connects each node of the top inverter with that of the bottom inverter through flying caps. The SOVD consists of an odd number of stages, with these top and bottom inverters and flying caps in one stage.

Fig. 2 shows the operation diagram of the SOVD in a steady state. When V_{IN} is applied to V_{MED}, the top and bottom ring oscillators oscillate; therefore, the voltage of each node switches between HIGH and LOW, as shown in Fig. 2. When n1 is HIGH, the operation is as shown on the left side of Fig. 2. During this operation, C_{FLY} is charged such that it has the same voltage as the input voltage. When n1 is LOW, the charged C_{FLY} and V_{IN} are switched in series, and V_{HIGH} is boosted to twice the voltage of V_{IN}.

Ideally, an SOVD has very low power consumption because these operations only transfer the charge of C_{FLY} to V_{HIGH}. However, a large leakage current will actually flow through the MOSFET, which should have been turned off, and power consumption will increase. Therefore, in the proposed SOVD, we will improve the power efficiency by reducing the leakage current of the MOSFETs that are turned off.

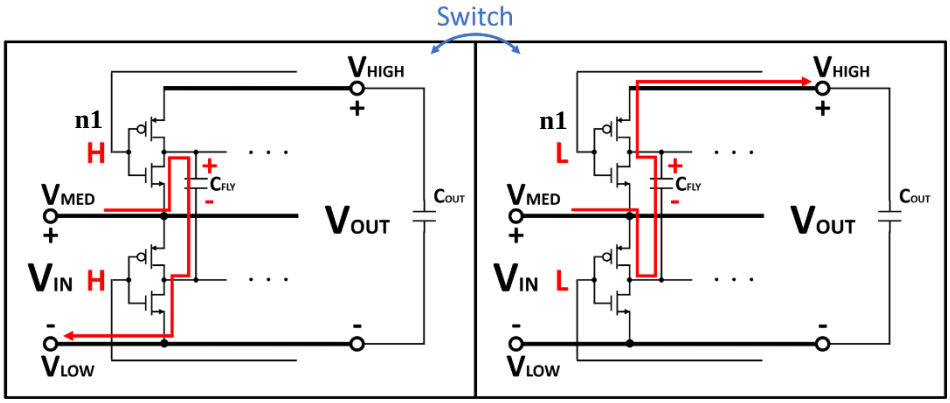

Fig. 2. Operation diagram of a conventional self-oscillating voltage doubler

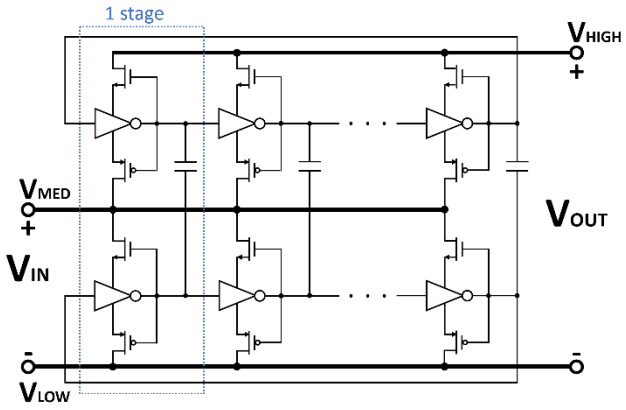

Fig. 3. Structure of the proposed self-oscillating voltage doubler

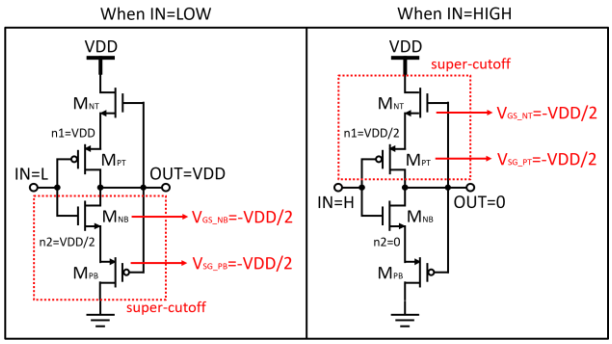

Fig. 4. Operation of a dynamic leakage-suppression inverter

B. Proposed self-oscillating voltage doubler

Fig. 3 demonstrates the structure of the proposed SOVD. As shown in Fig. 3, the proposed SOVD adds two MOSFETs above and below the basic inverter, and the output of the inverter is fed back to the input of these MOSFETs. These additional MOSFETs should have a lower threshold voltage than the MOSFETs of the inverter such that they can respond quickly to output fluctuations. Because this structure can operate dynamically to reduce the leakage current in response to input fluctuations, it is called dynamic leakage-suppression logic (DLS logic).

The detailed operations of the DLS inverter are described with reference to Fig. 4 (reference [5]). Assuming that the output node has no charge in the initial state, M_{NB} and M_{PB} are turned ON when the input becomes HIGH. The voltage of n1 is approximately half the VDD because the output node is connected to the ground and becomes 0 V. At this time, because V_{GS} of M_{NT} and V_{SG} of M_{PT} are negative values, M_{NT} and M_{PT} are in a super-cutoff state. In the super-cutoff state, the leakage current decreases exponentially according to the following equation:

$$I_D = I_0 exp\left(\frac{V_{GS}}{\zeta V_T}\right) \quad (1)$$

Here, I_0 represents the current when V_{GS} is 0, V_T represents a temperature-dependent value, and ζ represents the deviation of the ideal force.

In contrast, when the input goes LOW, V_{GS} of M_{NB} and V_{SG} of M_{PB} are negative values, and M_{NB} and M_{PB} are placed in the super-cutoff state. Thus, the leakage current can be reduced.

Furthermore, the switching speed of the DLS inverter slows down because the DLS inverter feeds back the output. Therefore, the proposed SOVD can slow down the oscillation frequency and reduce switching loss in circuits that do not require a high oscillation frequency.

III. SIMULATION RESULT

The conventional SOVD and the proposed SOVD were compared by spice simulation based on a standard 22 nm CMOS technology. V_{IN} was simulated at 200 mV to 400 mV, assuming an on-chip photodiode (reference [1]). When V_{IN} was changed, V_{HIGH}, the leakage current, and oscillation frequency are as shown in Fig. 5. The leakage current is the total current that flows to V_{LOW}.

In the conventional SOVD, the leakage current increases exponentially with respect to V_{IN}. This is because the output of the inverter does not become completely zero, and V_{GS} does not become zero even when the n-MOS is on because the actual MOSFET has an on-resistance. Thus, the leakage current increases exponentially according to Equation (1). However, in the proposed SOVD, the leakage current was significantly reduced because DLS logic dynamically created

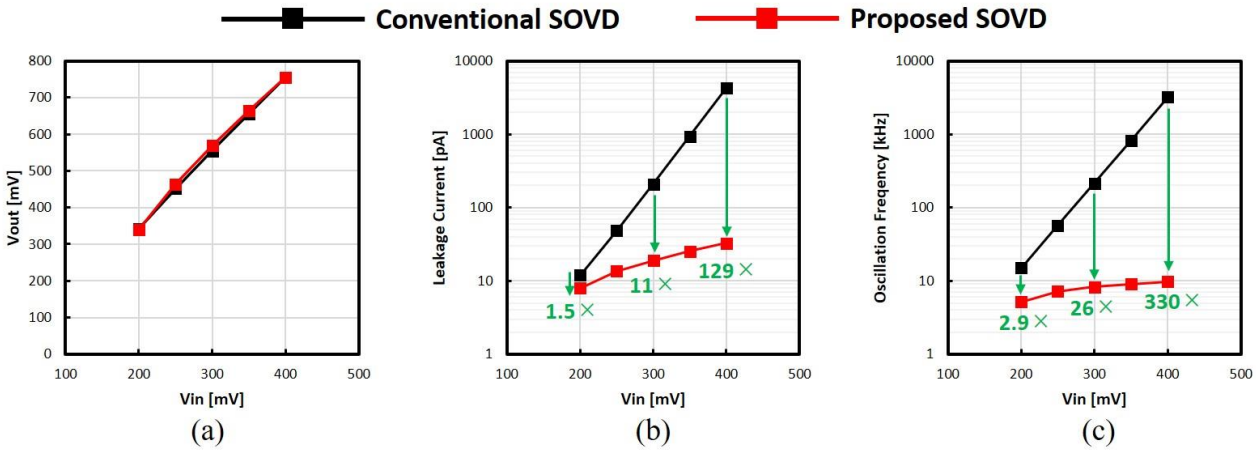

Fig. 5. Simulation results: (a) $V_{IN} - V_{OUT}$ characteristics, (b) $V_{IN} - I_{off}$ characteristics, and (c) $V_{IN} - f_{OSC}$ characteristics

TABLE I. PERFORMANCE COMPARISON BY SPICE SIMULATION

	Conventional SOVD	Proposed SOVD
Technology	22nm CMOS	22nm CMOS
Architecture	5 chains SOVD with basic CMOS inverter	5 chains SOVD with DLS inverter
Area	29.0 × 20.3 µm	29.0 × 33.8 µm
Input voltage	300mV	300mV
Output voltage	554.5 mV	568.6 mV
Leakage current	210.0 pA	19.0 pA
Oscillation frequency	1062.7 kHz	40.9 kHz
Power efficiency	4.5%	31.4%

V_{GS} a negative value. Furthermore, the oscillation frequency was also suppressed from a rapid increase owing to the feedback structure of the DLS inverter.

TABLE I presents a performance comparison when V_{IN} is 300 mV. The leakage current of the proposed SOVD reduced by 91.0% compared with the conventional one. Therefore, the power efficiency improved by 26.9%, which was about 7 times. Moreover, the oscillation frequency of the proposed SOVD reduced by 96.1%, and a considerable reduction in the switching loss could be expected. From these performance comparison results, it was possible to demonstrate the low power consumption of the proposed SOVD.

IV. CONCLUSION

In this study, we designed a new SOVD with a standard 22 nm CMOS technology that achieved low power consumption. Because the on-chip photodiode is about 300 mV in an illuminated office environment (200 lx), the leakage current can be reduced by 91.0% or more, and the oscillation frequency can be reduced by 96.1% or more if the proposed SOVD is used in a brighter place than the illuminated office environment. Therefore, if the proposed SOVD is mounted on a device used in such environments without requiring a high-speed oscillation frequency, an efficient device can be realized.

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